V. APPENDIX

Let the Y-parameters of networks A and B in Fig. 2 be

$$\boldsymbol{Y_A} = \left[\begin{array}{c|c} \boldsymbol{Y_{Am}} & \boldsymbol{y_A^T} \\ \hline \boldsymbol{y_A} & Y_{Ann} \end{array}\right] \quad \text{and}$$

$$\boldsymbol{Y_B} = \left[\begin{array}{c|c} \boldsymbol{Y_{Bm}} & \boldsymbol{y_B^T} \\ \hline \boldsymbol{y_B} & Y_{Bnn} \end{array}\right],$$

respectively, where

$$(\boldsymbol{Y_{Am}})_{i,j} = Y_{Aij}, \qquad (\boldsymbol{Y_{Bm}})_{i,j} = Y_{Bij},$$
$$1 \leqq i, \qquad j \leqq m,$$
$$\boldsymbol{y_A} = [Y_{A1n}, Y_{A2n}, \cdots, Y_{Amn}],$$
$$\boldsymbol{y_B} = [Y_{B1n}, Y_{B2n}, \cdots, Y_{Bmn}].$$

Denoting the Y-matrix of the k-th device $(1 \leqq k \leqq m)$ as

$$\begin{bmatrix} Y_{D11}^{(k)} & Y_{D12}^{(k)} \\ Y_{D21}^{(k)} & Y_{D22}^{(k)} \end{bmatrix},$$

we define matrices $\boldsymbol{Y_{D11}}$, $\boldsymbol{Y_{D12}}, \boldsymbol{Y_{D21}}$, and $\boldsymbol{Y_{D22}}$ by

$$\boldsymbol{Y_{Dij}} = \text{diag}\left[Y_{Dij}^{(1)}, Y_{Dij}^{(2)}, \cdots, Y_{Dij}^{(m)}\right], \qquad 1 \leqq i, \qquad j \leqq 2.$$

Then we obtain six equations similar to (1)–(6) in the text:

$$\boldsymbol{I_m} = \boldsymbol{Y_{Am}} \boldsymbol{V_m} + V_n \boldsymbol{y_A^T}, \tag{A1}$$

$$\boldsymbol{I'_m} = \boldsymbol{Y_{Bm}} \boldsymbol{V'_m} + V'_n \boldsymbol{y_B^T}, \tag{A2}$$

$$I_n = \boldsymbol{y_A} \boldsymbol{V_m} + V_n Y_{Ann}, \tag{A3}$$

$$I'_n = \boldsymbol{y_B} \boldsymbol{V'_m} + V'_n Y_{Bnn}, \tag{A4}$$

$$\boldsymbol{I_m} = -\boldsymbol{Y_{D11}} \boldsymbol{V_m} - \boldsymbol{Y_{D12}} \boldsymbol{V'_m}, \tag{A5}$$

$$\boldsymbol{I'_m} = -\boldsymbol{Y_{D21}} \boldsymbol{V_m} - \boldsymbol{Y_{D22}} \boldsymbol{V'_m}, \tag{A6}$$

where

$$\boldsymbol{I_m} = [I_1, I_2, \cdots, I_m]^T,$$
$$\boldsymbol{I'_m} = [I'_1, I'_2, \cdots, I'_m]^T,$$
$$\boldsymbol{V_m} = [V_1, V_2, \cdots, V_m]^T,$$
$$\boldsymbol{V'_m} = [V'_1, V'_2, \cdots, V'_m]^T.$$

From (A1)–(A6), the Y-parameters $(Y_{\text{I I}}, Y_{\text{I II}}, Y_{\text{II I}}, Y_{\text{II II}})$ in the text can be obtained.

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A Model for Coplanar Waveguide Transmission Line Structures on Semiconductor Substrates

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Abstract—**An accurate model for coplanar waveguide transmission line structures on semiconductive substrates is presented. The model is useful for simulating long (> 0.5 mm) interconnects on LSI and VLSI GaAs circuits as well as high speed Si ICs. When simulated in the frequency domain, the model shows an excellent match to measured S parameters of coplanar waveguide samples.**

I. INTRODUCTION

Since most GaAs integrated circuits are fabricated on semi-insulating substrates, the parasitic capacitances of interconnect lines to the backside RF ground plane are low. However, trends toward high density digital GaAs circuits result in closely spaced lines, and the interconnect parasitic capacitances from line to line are far more significant than those from line to distant ground plane. This would prompt us to treat long interconnects as coplanar waveguide (CPW) transmission lines, not as microstrip transmission lines [1]. The CPW lines are isolated from the back side ground plane and exhibit a quasi-TEM mode of propagation. Furthermore, in cases in which well controlled impedance characteristics are required, CPW lines can be produced by placing ground conductors adjacent to the signal lines.

A four element RLGC model is usually accurate for modelling CPW structures on semi-insulating GaAs, but not accurate when the structures are above a semiconductive substrate. Some digital GaAs MESFET processes, for example, incorporate p^- implants for threshold voltage control. If the implant layer extends below interconnect lines, as it would if the implant is not a selective one, signal propagation will be affected adversely by the presence of a lossy plane in close proximity to signal lines. This effect must be included in an accurate model.

This letter presents an accurate, physically intuitive model for simulating CPW structures above semiconductive substrates. The model is shown to be far superior to the simple four element RLGC model and significantly better than the model of reference [2].

II. MEASUREMENTS AND ANALYSIS

The test structures used for this study were 1 cm long CPW transmission lines whose cross section is depicted in Fig. 1. Line lengths were constrained to 1 cm by reticle size limitations. The samples were fabricated by Vitesse Semiconductor through the MOSIS foundry service [3]. The Vitesse process incorporates a nonselective

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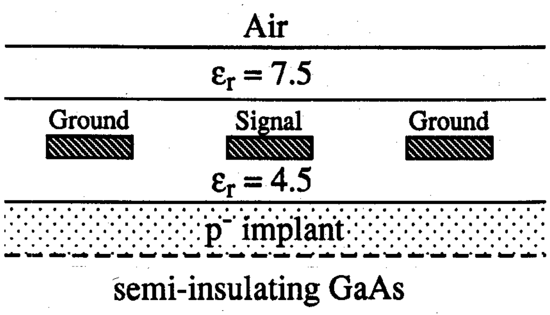


Fig. 1. Cross sectional view of CPW line structure on p^- implanted GaAs.

p^- implant. CPW structures were fabricated on the second and third metal levels which are typically used for long interconnects and power busses. The line spacings and widths were 6.4 μm and 3.2 μm respectively for metal two, and 5.6 μm and 5.6 μm for metal three. These widths and spacings were chosen because calculations assuming a highly conductive substrate indicated they would yield transmission lines with characteristic impedance near 50 Ω.

Scattering parameters were measured with coplanar probes from 45 MHz to 20 GHz. From the measured S parameter data, line parameters for the conventional four element transmission line model (Fig. 2a) were calculated [4]. The resulting parameters are depicted in Fig. 2 and are seen to be highly frequency dependent indicating that the simple four element model is not a good model of the CPW structures. In particular, the capacitance per unit length decreases rapidly from 45 MHz to about 3 GHz, and the resistance and conductance per unit length fluctuate wildly. The apparent inductance increase at low frequency is a consequence of limited phase accuracy on short samples.

The frequency variation of the line parameters extracted for the four element model can be understood by considering the resistance of the p^- layer and the capacitances of the signal and ground lines to the p^- layer. Fig. 3(a) illustrates the situation. The coupling from signal line through C_{PS}, R_{PT1} and R_{PT2}, and C_{PG1} and C_{PG2} to the ground lines must be considered in parallel with the coupling through the coplanar capacitances C_{COP1} and C_{COP2}.

III. Model Development

The development of a model for CPW lines on lossy substrates was achieved by matching the calculated S parameters of the physically intuitive model of Fig. 3(a) to measured S parameters. The model topology of Fig. 3(b) follows from the physical model of Fig. 3(a) where G_{PT} is the inverse of the parallel combination of R_{PT1} and R_{PT2}, and C_{PG} is the parallel combination of C_{PG1} and C_{PG2}. As usual, all element parameters are per unit length.

The CPW lines were modelled using identical series sections having the topology of Fig. 3(b). Fifty sections were used for each CPW structure. By comparing the results of the 50 section model to an 80 section model, it was verified that 50 sections were sufficient to model the lines. Initial values for R and L were obtained from the line parameters calculated for the four element model, whereas the initial value of C_{COP} was obtained from the high frequency capacitance of the four element model (Fig. 1). The p^- layer series resistance (R_{PL}) of the terminal sections was left floating, and a model of the probe pads was attached to each end of the CPW line model. The probe pad model also accounts for the conductivity of the substrate: it consists of a shunt 30 fF capacitor in parallel with the series combination of a 220 fF capacitor and 1880 Ω resistor. Initial estimates of the pad capacitances were obtained from the Vitesse Semiconductor design manual.

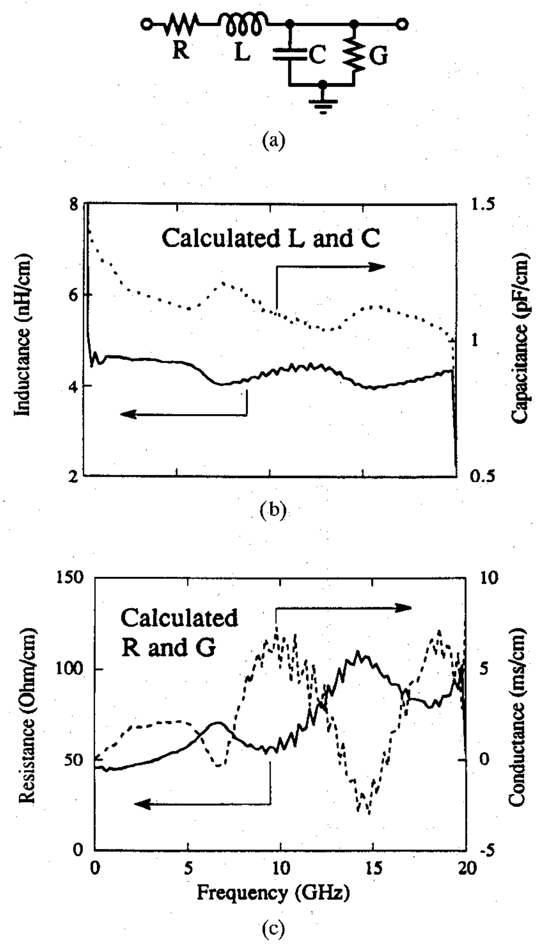


Fig. 2. Four element line parameters calculated form measured S parameters of metal 3 CPW line: (a) Inductance and capacitance, and (b) conductance and resistance.

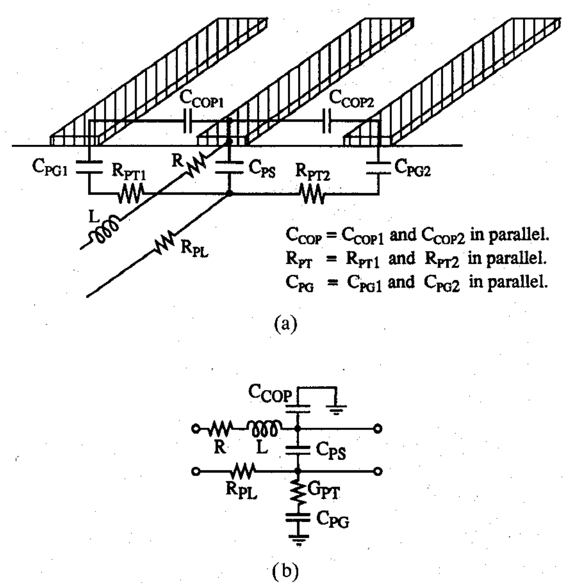
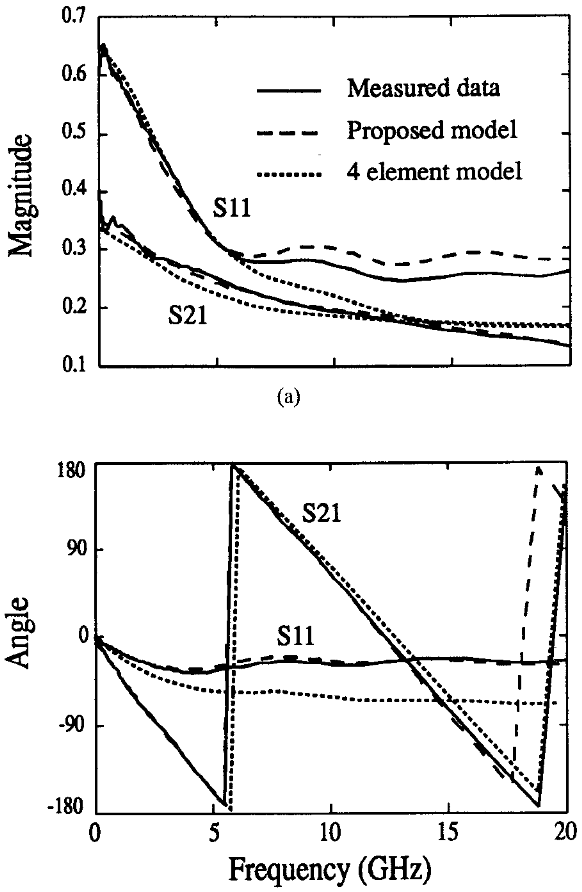


Fig. 3. (a) Physically intuitive model including p^- layer effects, and (b) simplified 4-port model.

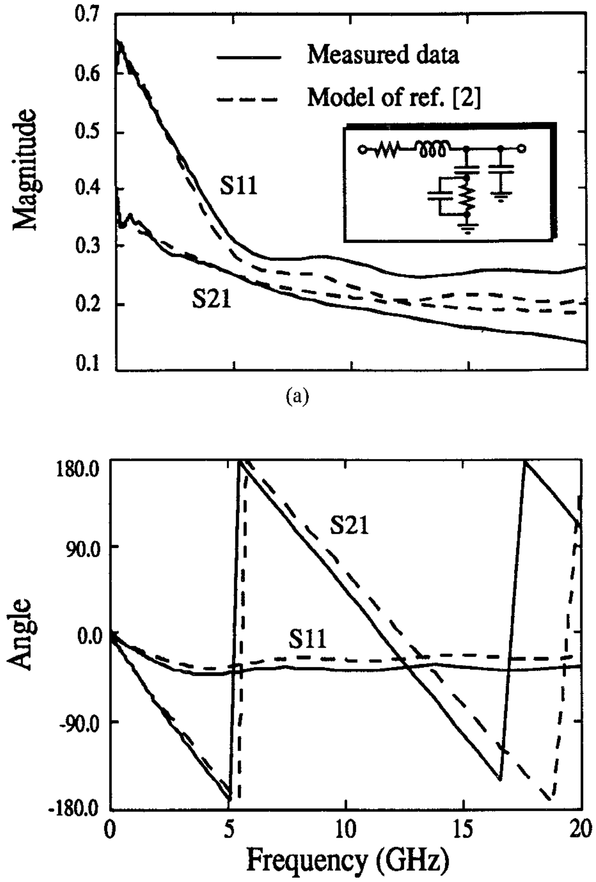
Using a frequency domain simulator (LIBRA [5]), the element values of the line model were tuned to achieve the best match between



(a)

(b)

Fig. 4. $S11$ and $S12$ magnitude (a) and phase angle (b) of proposed line model (solid), measured metal 2 CPW line (dashed) and conventional four element RLGC model (dotted). Inadequacy of four element model is apparent.



(a)

(b)

Fig. 5. $S11$ and $S12$ magnitude (a) and phase angle (b) of measured metal 3 CPW line (solid) and the model of reference [2] shown in inset of 5(a). Model of Fig. 3 is seen to fit measured data considerably better (see Fig. 4).

TABLE I
ELEMENT VALUES OF THE PROPOSED MODEL WHICH PROVIDE THE CLOSEST MATCH OF THE MODELLED TO THE MEASURED S PARAMETERS OF METAL 2 AND METAL 3 LINE SAMPLES

Element	Metal 2 CPW	Metal 3 CPW
L	6.9 nH/cm	4.6 nH/cm
C_{COP}	870 fF/cm	915 fF/cm
C_{PS}	460 fF/cm	342 fF/cm
C_{PG}	1.34 pF/cm	1.30 pF/cm
R	186 Ω/cm	49 Ω/cm
R_{PL}	9750 Ω/cm	8310 Ω/cm
G_{PT}	9.3 mS/cm	9.2 mS/cm

modelled and measured S parameters. The element values which provide the closest match of modelled and measured S parameters are summarized in Table I. The resulting match for the second metal CPW line is shown in Fig. 4. For comparison, the best match to a 50 section, four element RLGC model is also plotted in Fig. 4.

The authors of reference [6] proposed a simple modification to the four element RLGC to model transmission lines on heavily doped semiconductor substrates: a resistor in parallel with the series inductor and resistor to represent losses in the semiconductor. Attempts to match the measured data to this model yielded somewhat better results than the four element RLGC, but good matches to both the amplitudes and phases of $S21$ and $S11$ were not possible.

The model proposed in this paper was also compared to that proposed by Pribetich, *et al.* in [2]. Though the Pribetich model could be tuned to fit the measured data of the metal three CPW lines almost as well as the model we propose, its best fit to the metal 2 line was significantly worse, especially above 6 GHz. The best match of the Pribetich model to the measured S parameters of the second metal CPW line is shown in Fig. 5.

IV. CONCLUSION

An accurate model has been developed for long interconnect lines over a lossy substrate. Its effectiveness on GaAs substrates has been shown, and it should also apply to lines on silicon ICs. While the model is quite accurate for the CPW structures measured in this work, scaling rules for lines of different widths and spacings on substrates of different conductivity have yet to be developed.

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